Dual Ultralow Distortion, Differential ADC Driver

Preliminary Technical Data

ADA4937-2

FEATURES

- **Extremely low harmonic distortion**
  - **−112 dBc HD2 @ 10 MHz**
  - **−79 dBc HD2 @ 70 MHz**
  - **−70 dBc HD2 @ 100 MHz**
  - **−102 dBc HD3 @ 10 MHz**
  - **−91 dBc HD3 @ 70 MHz**
  - **−84 dBc HD3 @ 100 MHz**
- **Low input voltage noise: 2.2 nV/√Hz**
- **High speed**
  - **−3 dB bandwidth of 1.9 GHz, G = 1**
  - **Slew rate: 6000 V/µs, 25% to 75%**
  - **0.1 dB gain flatness to 200 MHz**
  - **Fast overdrive recovery of 1 ns**
- **1 mV typical offset voltage**
- **Externally adjustable gain**
- **Differential-to-differential or single-ended-to-differential operation**
- **Adjustable output common-mode voltage**
- **Single-supply operation: 3.3 V to 5 V**
- **Pb-free, 4 mm × 4 mm 24-lead LFCSP**

APPLICATIONS

- **ADC drivers**
- **Single-ended-to-differential converters**
- **IF and baseband gain blocks**
- **Differential buffers**
- **Line drivers**

FUNCTIONAL BLOCK DIAGRAM

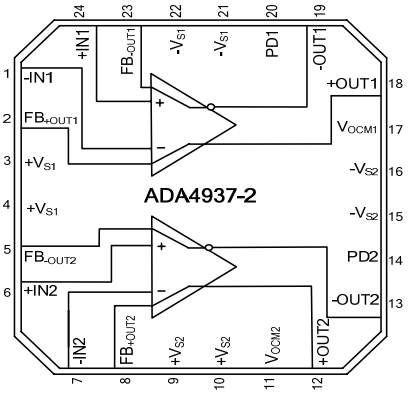

Figure 1.

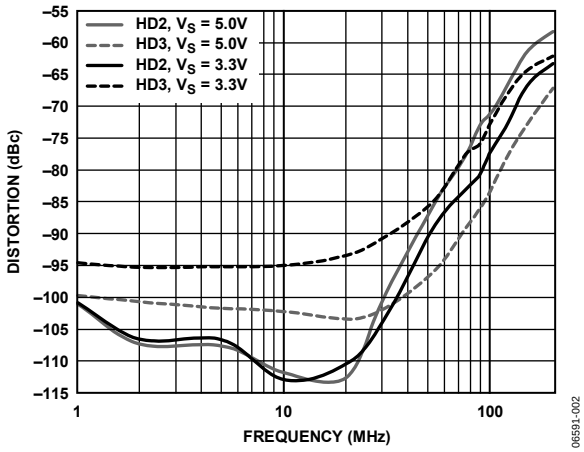

Figure 2. Harmonic Distortion vs. Frequency

GENERAL DESCRIPTION

The ADA4937-2 is a dual low noise, ultralow distortion, high-speed differential amplifier. It is an ideal choice for driving high performance ADCs with resolutions up to 16 bits from dc to 100 MHz. The adjustable level of the output common mode allows the ADA4937-2 to match the input of the ADC. The internal common-mode feedback loop also provides exceptional output balance as well as suppression of even-order harmonic distortion products.

With the ADA4937-2, differential gain configurations are easily realized with a simple external feedback network of four resistors determining the closed-loop gain of each amplifier.

The ADA4937-2 is fabricated using Analog Devices, Inc. proprietary silicon-germanium (SiGe), complementary bipolar process, enabling it to achieve very low levels of distortion with an input voltage noise of only 2.2 nV/√Hz. The low dc offset and excellent dynamic performance of the ADA4937-2 make it well suited for a wide variety of data acquisition and signal processing applications.

The ADA4937-2 is available in a Pb-free, 4 mm × 4 mm 24-lead LFCSP. The pinout has been optimized to facilitate PCB layout and minimize distortion. The part is specified to operate over the −40°C to +105°C temperature range for 3.3 V supplies and the −40°C to +85°C temperature range for 5 V supplies.

Rev. PrA

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REVISION HISTORY

7/30—Revision PrA: Initial Version

Rev. PrA

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SPECIFICATIONS

5 V OPERATION

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, V_{OCM} = $+V_S$ /2, R_T = 61.9 Ω, R_G = R_F = 200 Ω, G = 1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted.
All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 1. ±D_{IN} to ±OUT Performance

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 0.1 V p-p		1900		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 0.1 V p-p		200		MHz
Large Signal Bandwidth	$V_{OUT, dm}$ = 2 V p-p		1700		MHz
Slew Rate	$V_{OUT, dm}$ = 2 V p-p; 25% to 75%		6000		V/µs
Overdrive Recovery Time	V_{IN} = 0 V to 1.5 V step; G = 3.16		<1		ns
NOISE/HARMONIC PERFORMANCE	See Figure 45 for distortion test circuit				
Second Harmonic	$V_{OUT, dm}$ = 2 V p-p; 10 MHz		−112		dBc
	$V_{OUT, dm}$ = 2 V p-p;, 70 MHz		−79		dBc
	$V_{OUT, dm}$ = 2 V p-p; 100 MHz		−70		dBc
Third Harmonic	$V_{OUT, dm}$ = 2 V p-p; 10 MHz		−102		dBc
	$V_{OUT, dm}$ = 2 V p-p; 70 MHz		−91		dBc
	$V_{OUT, dm}$ = 2 V p-p; 100 MHz		−84		dBc
IMD	f_1 = 70 MHz; f_2 = 70.1 MHz; $V_{OUT, dm}$ = 2 V p-p		−91		dBc
Voltage Noise (RTI)	f = 100 kHz		2.2		nV/√Hz
Input Current Noise	f = 100 kHz		3		pA/√Hz
Noise Figure	G = 4; R_T = 136 Ω; R_F = 200 Ω; R_G = 37 Ω; f = 100 MHz		15		dB
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = V_{DIN-} = 2.5 V	−2.5	+0.5	+2.5	mV
	T_{MIN} to T_{MAX} variation		±1		µV/°C
Input Bias Current		−30	−20	−10	µA
	T_{MIN} to T_{MAX} variation		0.01		µA/°C
Input Offset Current		−2	+0.5	+2	µA
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			0.3 to 3.0		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1 V	−67	−80		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output; R_F = R_G = 10 kΩ	0.8		4.2	V
Linear Output Current			>100		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V; 10 MHz; see Figure 44 for test circuit		−61		dB

Table 2. V_{OCM} to ±OUT Performance

Parameter	Conditions	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth			440		MHz
Slew Rate	V_{IN} = 1.5 V to 3.5 V; 25% to 75%		1150		V/µs
Input Voltage Noise (RTI)	f = 100 kHz		7.5		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		1.2		3.8	V
Input Resistance		8	10	12	kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-} = +V_S/2$		2	6.1	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−75		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.97	0.98	1.00	V/V
POWER SUPPLY					
Operating Range		3.0		5.25	V
Quiescent Current		TBD	TBD	TBD	mA
	T_{MIN} to T_{MAX} variation		17		µA/°C
	Powered down	0.02	0.3	0.4	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = 1 V	−70	−90		dB
POWER DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤1		V
	Enabled		≥2		V
Turn-Off Time			1		µs
Turn-On Time			200		Ns
$\overline{PD}$ Bias Current					
Enabled	$\overline{PD}$ = 5 V	10	40	50	µA
Disabled	$\overline{PD}$ = 0 V	−300	−200	−150	µA
OPERATING TEMPERATURE RANGE		−40		+85	°C

3.3 V OPERATION

T_A = 25°C, $+V_S$ = 3.3 V, $-V_S$ = 0 V, V_{OCM} = $+V_S$ /2, R_T = 61.9 Ω, R_G = R_F = 200 Ω, G = 1, $R_{L, dm}$ = 1 kΩ, unless otherwise noted. All specifications refer to single-ended input and differential outputs, unless otherwise noted.

Table 3. ±D_{IN} to ±OUT Performance

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{OUT, dm}$ = 0.1 V p-p		1900		MHz
Bandwidth for 0.1 dB Flatness	$V_{OUT, dm}$ = 0.1 V p-p		200		MHz
Large Signal Bandwidth	$V_{OUT, dm}$= 2 V p-p		1300		MHz
Slew Rate	$V_{OUT, dm}$ = 2 V p-p; 25% to 75%		4000		V/µs
Overdrive Recovery Time	V_{IN} = 0 V to 1.0 V step; G = 3.16		<1		ns
NOISE/HARMONIC PERFORMANCE	See Figure 45 for distortion test circuit				
Second Harmonic	$V_{OUT, dm}$ = 2 V p-p; 10 MHz		−106		dBc
	$V_{OUT, dm}$ = 2 V p-p; 70 MHz		−88		dBc
	$V_{OUT, dm}$ = 2 V p-p; 100 MHz		−81		dBc
Third Harmonic	$V_{OUT, dm}$ = 2 V p-p; 10 MHz		−93		dBc
	$V_{OUT, dm}$ = 2 V p-p; 70 MHz		−80		dBc
	$V_{OUT, dm}$ = 2 V p-p; 100 MHz		−71		dBc
IMD	f_1 = 70 MHz; f_2 = 70.1 MHz; $V_{OUT, dm}$ = 2 V p-p		−87		dBc
Voltage Noise (RTI)	f = 100 kHz		2.2		nV/√Hz
Input Current Noise	f = 100 kHz		3		pA/√Hz
Noise Figure	G = 4; R_T = 136 Ω; R_F = 200 Ω; R_G = 37 Ω; f = 100 MHz		15		dB
INPUT CHARACTERISTICS					
Offset Voltage	$V_{OS, dm}$ = $V_{OUT, dm}$/2; V_{DIN+} = V_{DIN-} = $+V_S$/2	−2.5	+0.5	+2.5	mV
	T_{MIN} to T_{MAX} variation		±1		µV/°C
Input Bias Current		−50	−20	−10	µA
	T_{MIN} to T_{MAX} variation		0.01		µA/°C
Input Resistance	Differential		6		MΩ
	Common mode		3		MΩ
Input Capacitance			1		pF
Input Common-Mode Voltage			0.3 to 1.2		V
CMRR	$\Delta V_{OUT, dm}/\Delta V_{IN, cm}$; $\Delta V_{IN, cm}$ = ±1.0 V	−67	−80		dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing	Maximum ΔV_{OUT}; single-ended output	0.8		2.5	V
Linear Output Current			95		mA
Output Balance Error	$\Delta V_{OUT, cm}/\Delta V_{OUT, dm}$; $\Delta V_{OUT, dm}$ = 1 V; f = 10 MHz; see Figure 44 for test circuit		−61		dB

Table 4. V_{OCM} to ±OUT Performance

Parameter	Conditions	Min	Typ	Max	Unit
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth			440		MHz
Slew Rate	V_{IN} = 0.9 V to 2.4 V; 25% to 75%		900		V/µs
Input Voltage Noise (RTI)	f = 100 kHz		7.5		nV/√Hz
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range		1.2		2.1	V
Input Resistance			10		kΩ
Input Offset Voltage	$V_{OS, cm} = V_{OUT, cm}$; $V_{DIN+} = V_{DIN-}$ = 1.67 V		2	6.1	mV
Input Bias Current			0.5		µA
V_{OCM} CMRR	$\Delta V_{OUT, dm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V		−75		dB
Gain	$\Delta V_{OUT, cm}/\Delta V_{OCM}$; ΔV_{OCM} = ±1 V	0.97	0.98	1.00	V/V
POWER SUPPLY					
Operating Range		3.0		5.25	V
Quiescent Current		TBD	TBD	TBD	mA
	T_{MIN} to T_{MAX} variation		17		µA/°C
	Powered down	0.02	0.2	0.3	mA
Power Supply Rejection Ratio	$\Delta V_{OUT, dm}/\Delta V_S$; ΔV_S = 1 V	−70	−90		dB
POWER DOWN ($\overline{PD}$)					
$\overline{PD}$ Input Voltage	Powered down		≤1		V
	Enabled		≥2		V
Turn-Off Time			1		µs
Turn-On Time			200		Ns
$\overline{PD}$ Bias Current					
Enabled	$\overline{PD}$ = 3.3 V	10	20	30	µA
Disabled	$\overline{PD}$ = 0 V	−200	−120	−100	µA
OPERATING TEMPERATURE RANGE		−40		+105	°C

ABSOLUTE MAXIMUM RATINGS

Table 5.

Parameter	Rating
Supply Voltage	5.5 V
Power Dissipation	See Figure 3
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +TBD°C
Lead Temperature (Soldering, 10 sec)	300°C
Junction Temperature	TBD°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the device (including exposed pad) soldered to a high thermal conductivity 2s2p circuit board, as described in EIA/JESD 51-7.

Table 6. Thermal Resistance

Package Type	θ_{JA}	Unit
24-Lead LFCSP (Exposed Pad)	TBD	°C/W

Maximum Power Dissipation

The maximum safe power dissipation in the ADA4937-2 package is limited by the associated rise in junction temperature (T_J) on the die. At approximately TBD°C, which is the glass transition temperature, the plastic changes its properties. Even temporarily exceeding this temperature limit can change the stresses that the package exerts on the die, permanently shifting the parametric performance of the ADA4937-2. Exceeding a junction temperature of 150°C for an extended period can result in changes in the silicon devices, potentially causing failure.

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). The power dissipated due to the load drive depends upon the particular application. The power due to load drive is calculated by multiplying the load current by the associated voltage drop across the device. RMS voltages and currents must be used in these calculations.

Airflow increases heat dissipation, effectively reducing θ_{JA}. In addition, more metal directly in contact with the package leads/exposed pad from metal traces, through holes, ground, and power planes reduces the θ_{JA}.

Figure 3 shows the maximum safe power dissipation in the package vs. the ambient temperature for the 24-lead LFCSP (TBD°C/W) on a JEDEC standard 4-layer board.

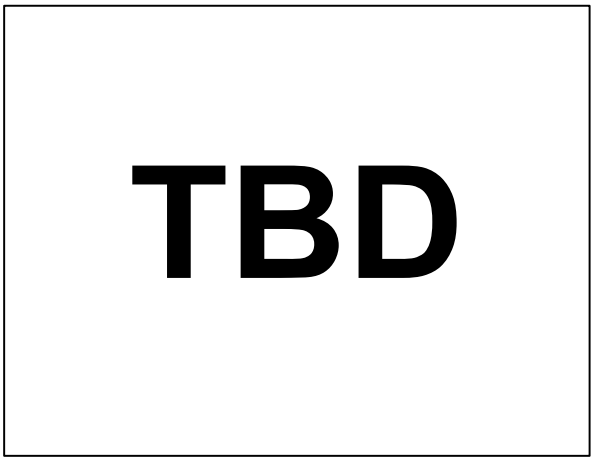


Figure 3. Maximum Power Dissipation vs. Temperature for a 4-Layer Board

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

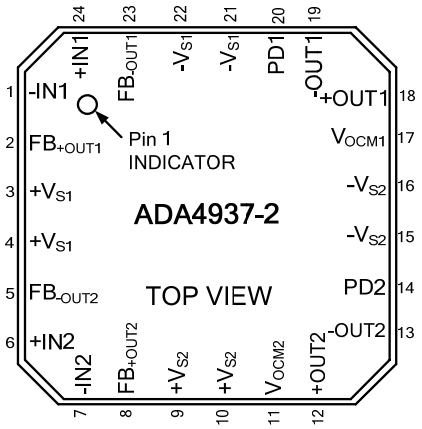


Figure 4. Pin Configuration

Table 7. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	–IN1	Negative input summing node 1
2	FB_{+OUT1}	Positive output feedback pin 1
3, 4	$+V_{S1}$	Positive supply voltage 1
5	FB_{-OUT2}	Negative output feedback pin 2
6	+IN2	Positive input summing node 2
7	–IN2	Negative input summing node 2
8	FB_{+OUT2}	Positive output feedback pin 2
9, 10	$+V_{S2}$	Positive supply voltage 2
11	V_{OCM2}	Output common mode voltage 2
12	+OUT2	Positive output 2
13	–OUT2	Negative output 2
14	PD2	Power-down pin 2
15, 16	$–V_{S2}$	Negative supply voltage 2
17	V_{OCM1}	Output common mode voltage 1
18	+OUT1	Positive output 1
19	–OUT1	Negative output 1
20	PD1	Power-down pin 1
21, 22	$–V_{S1}$	Negative supply voltage 1
23	FB_{-OUT1}	Negative output feedback pin 1
24	+IN1	Positive input summing node 1

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, $+V_S$ = 5 V, $-V_S$ = 0 V, $V_{OUT,dm}$ = 2 V p-p, V_{OCM} = $+V_S$ /2, R_T = 61.9 Ω, R_G = R_F = 200 Ω, G = 1, $R_{L,dm}$ = 1 kΩ, unless otherwise noted. Refer to Figure 43 for test setup.

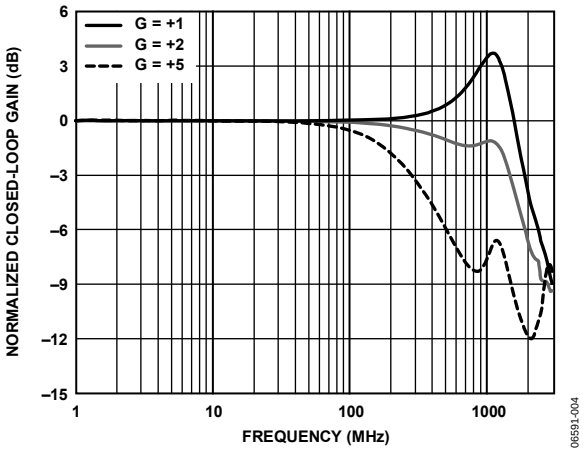


Figure 5. Small Signal Frequency Response for Various Gains, $V_{OUT,dm}$ = 100 mV p-p

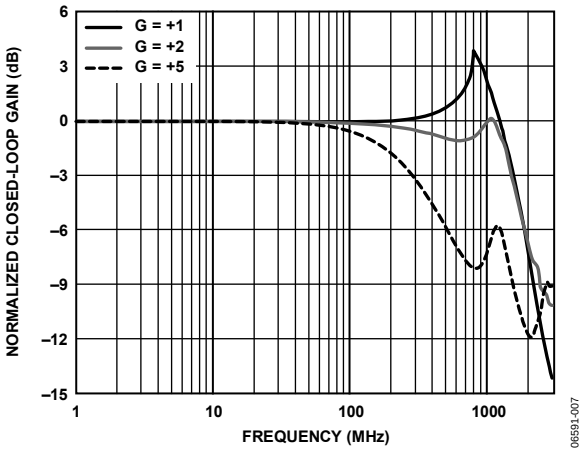


Figure 8. Large Signal Frequency Response for Various Gains

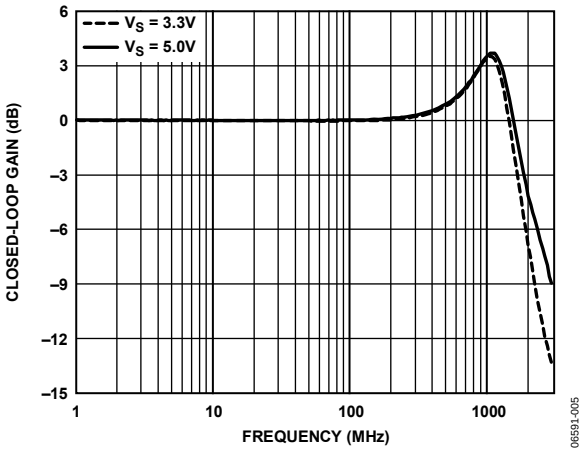


Figure 6. Small Signal Frequency Response for Various Supplies, $V_{OUT,dm}$ = 100 mV p-p

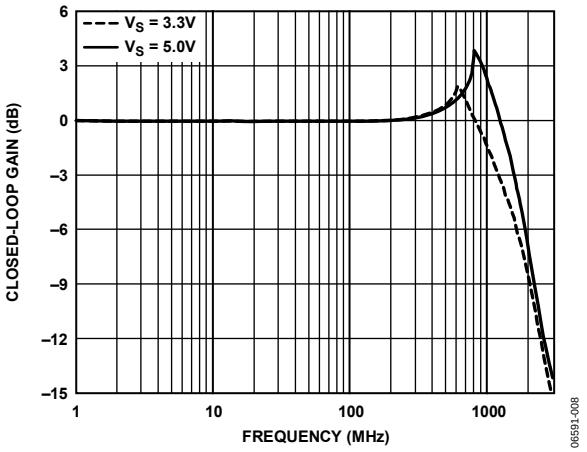


Figure 9. Large Signal Frequency Response for Various Supplies

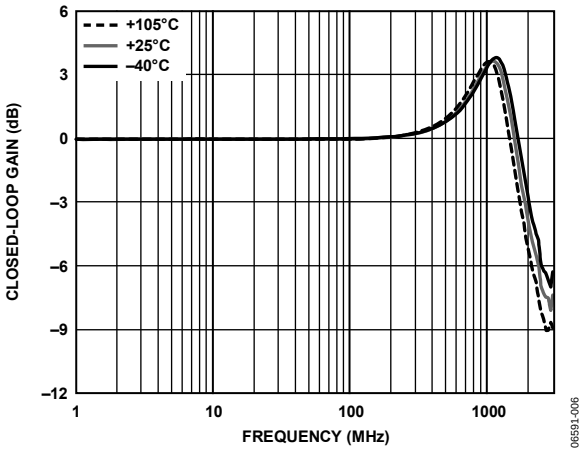


Figure 7. Small Signal Frequency Response for Various Temperatures, $V_{OUT,dm}$ = 100 mV p-p

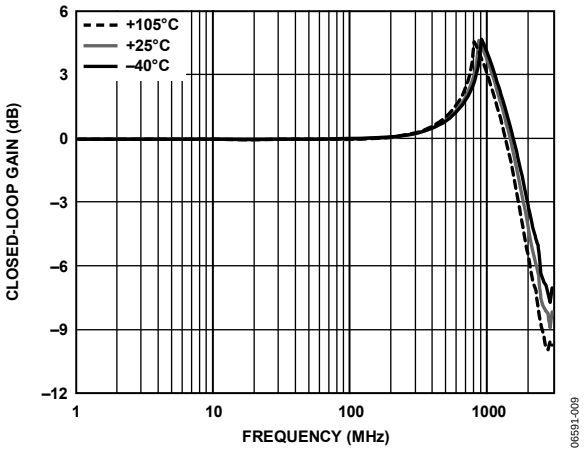


Figure 10. Large Signal Frequency Response for Various Temperatures

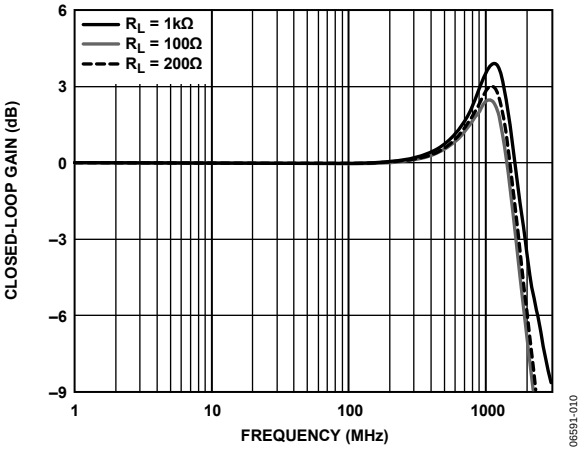


Figure 11. Small Signal Frequency Response for Various Loads, $V_{OUT, dm}$ = 100 mV p-p

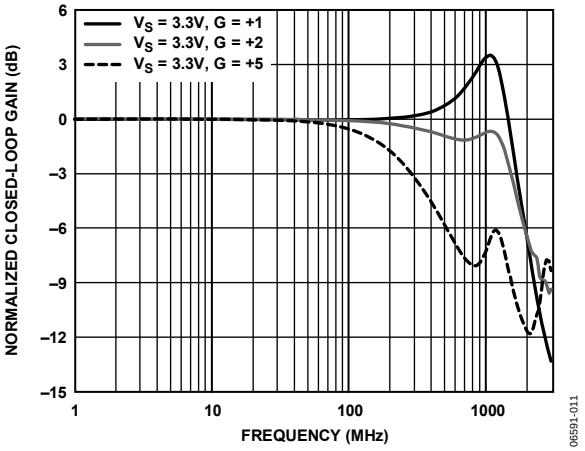


Figure 12. Small Signal Frequency Response for Various Gains, V_S = 3.3 V and $V_{OUT, dm}$ = 100 mV p-p

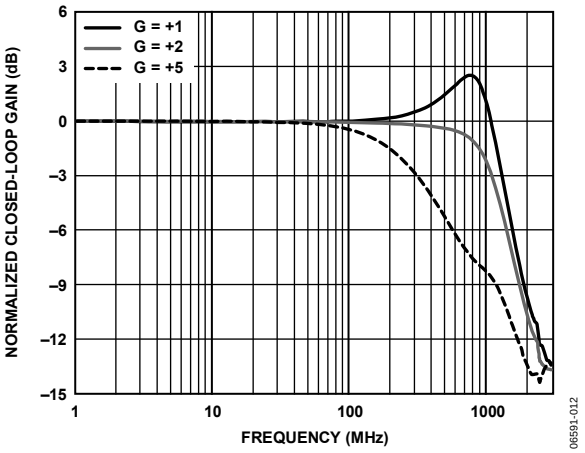


Figure 13. Small Signal Frequency Response for Various Gains, $V_{OUT, dm}$ = 100 mV p-p, R_F = 348 Ω

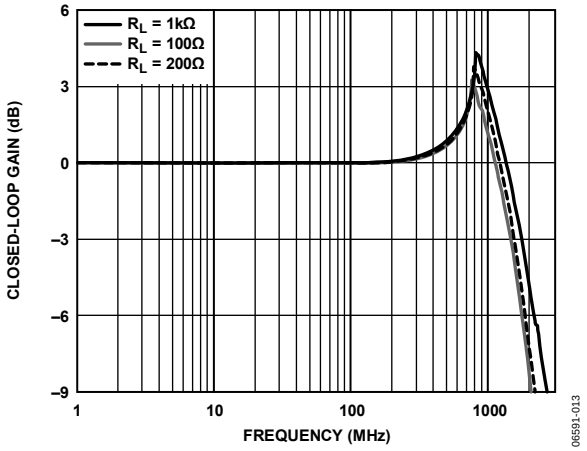


Figure 14. Large Signal Frequency Response for Various Loads

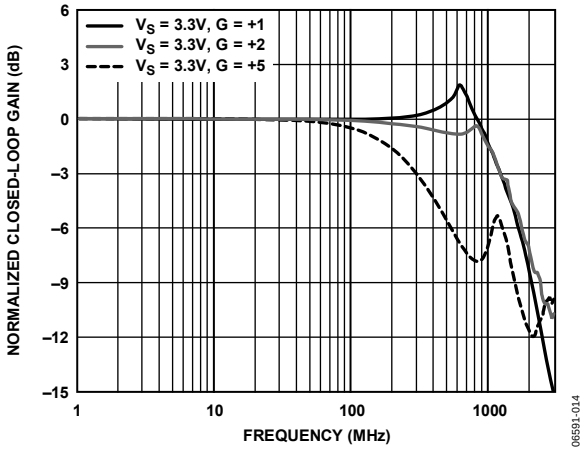


Figure 15. Large Signal Frequency Response for Various Gains, V_S = 3.3 V

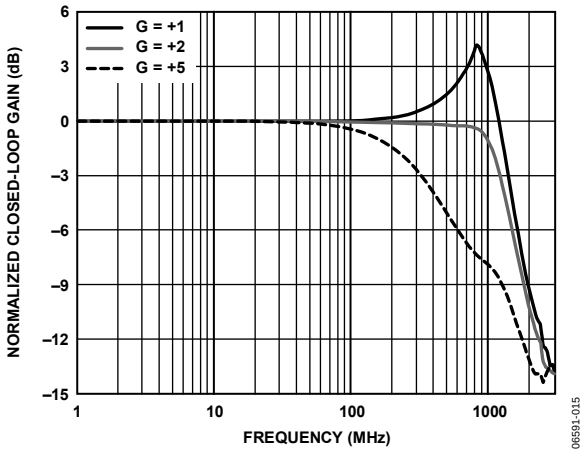


Figure 16. Large Signal Frequency Response for Various Gains, R_F = 348 Ω

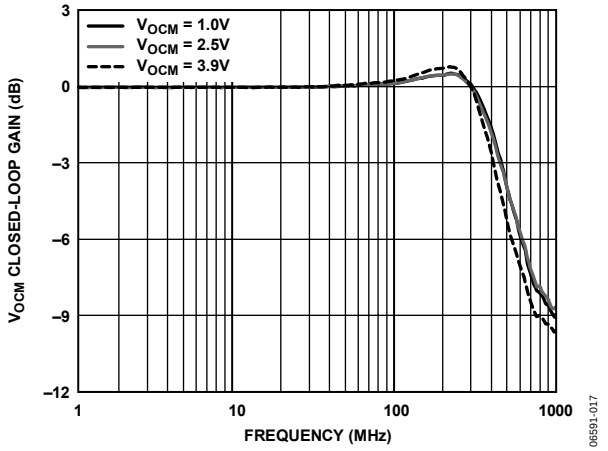


Figure 17. Small Signal Frequency Response for Various V_{OCM}

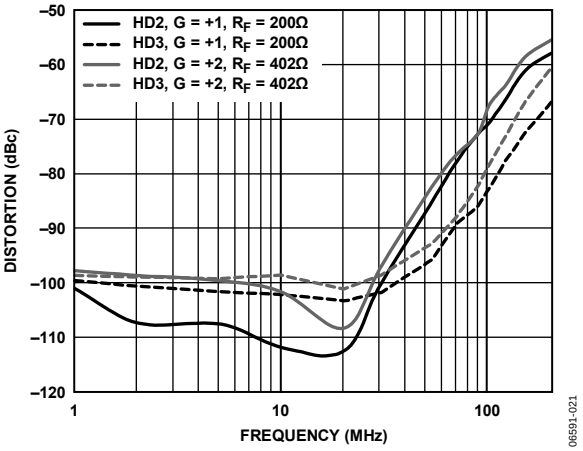


Figure 20. Harmonic Distortion vs. Frequency and Gain

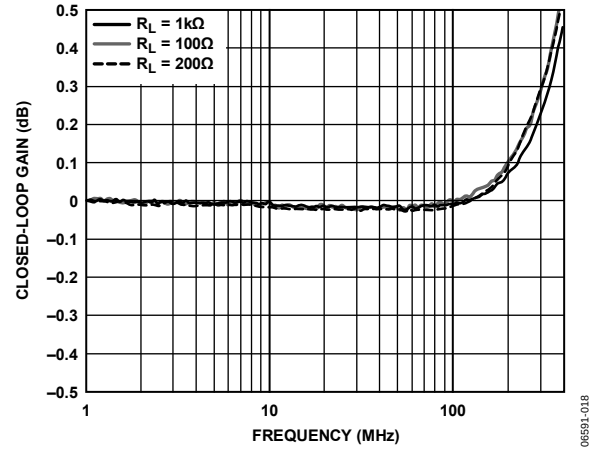


Figure 18. 0.1 dB Flatness Response for Various Loads

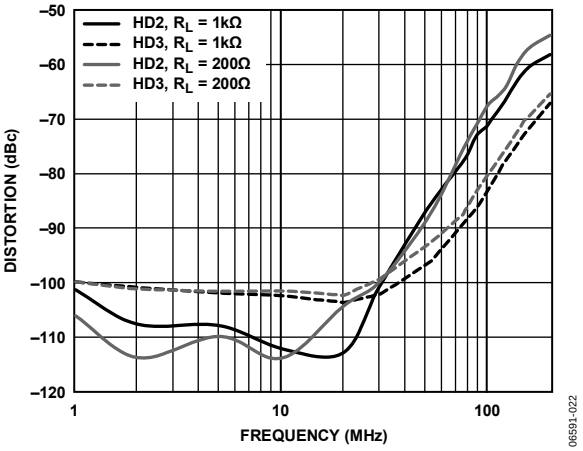


Figure 21. Harmonic Distortion vs. Frequency and Load

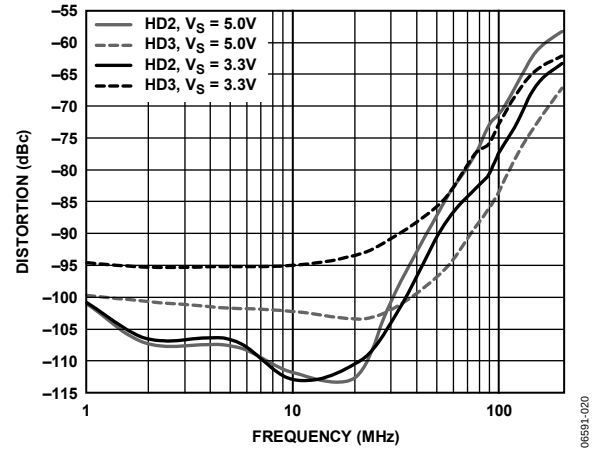


Figure 19. Harmonic Distortion vs. Frequency and Supply Voltage

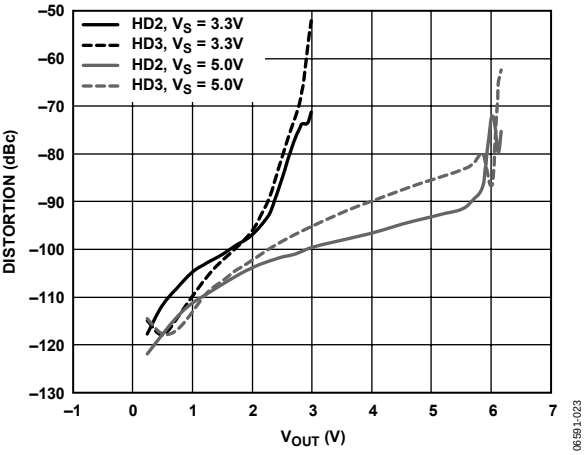


Figure 22. Harmonic Distortion vs. V_{OUT} and Supply Voltage

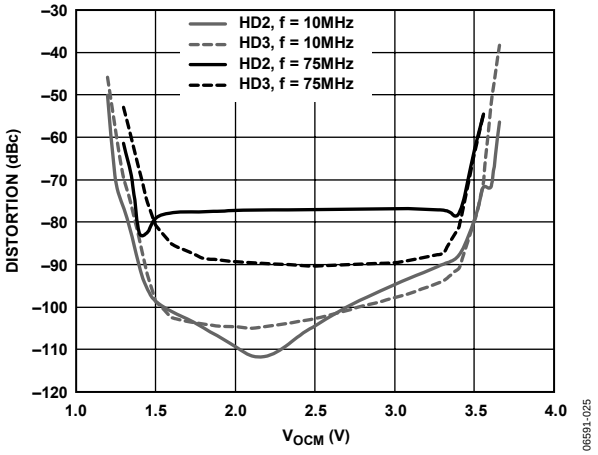


Figure 23. Harmonic Distortion vs. V_{OCM} and Frequency

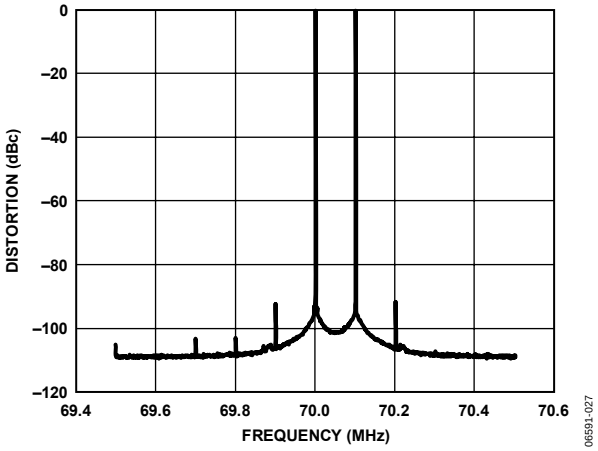


Figure 26. 70 MHz Intermodulation Distortion

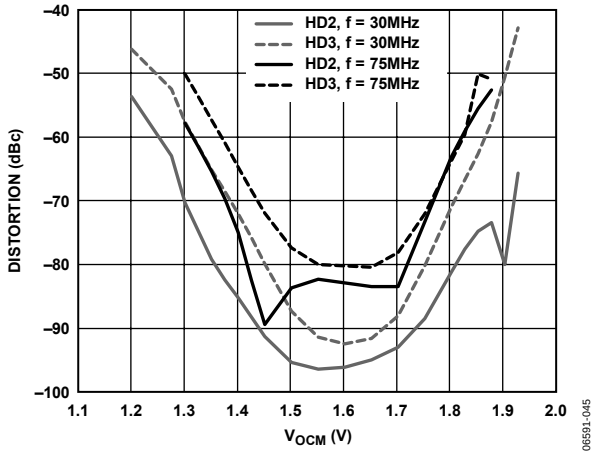


Figure 24. Harmonic Distortion vs. V_{OCM} and Frequency, V_S = 3.3 V

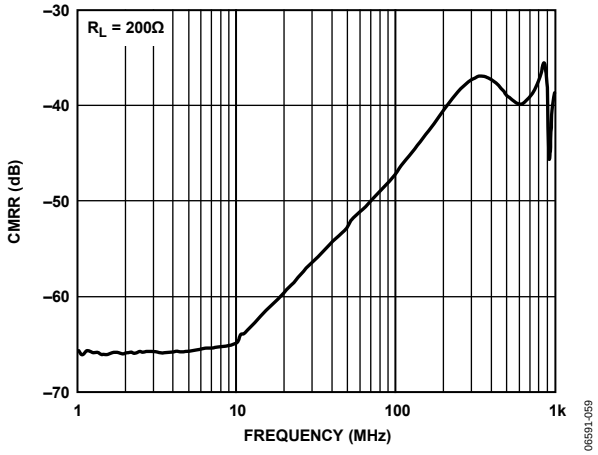


Figure 27. CMRR vs. Frequency

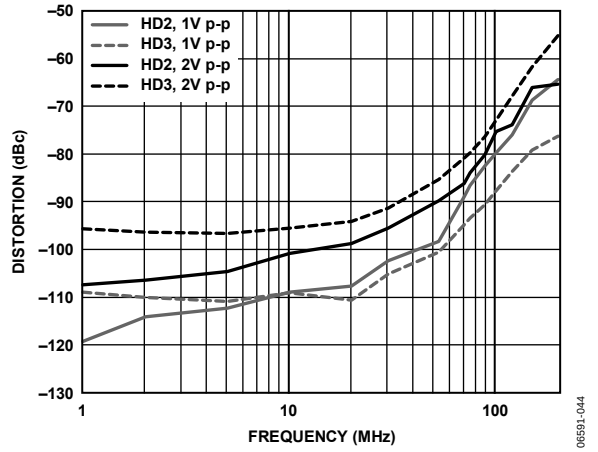


Figure 25. Harmonic Distortion vs. Frequency and V_{OUT}, V_S = 3.3 V

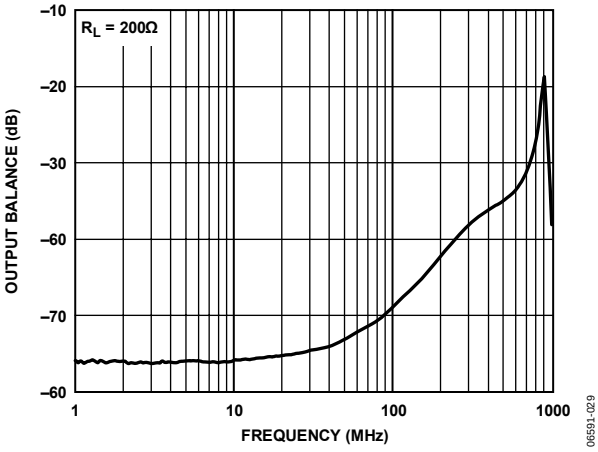


Figure 28. Output Balance vs. Frequency

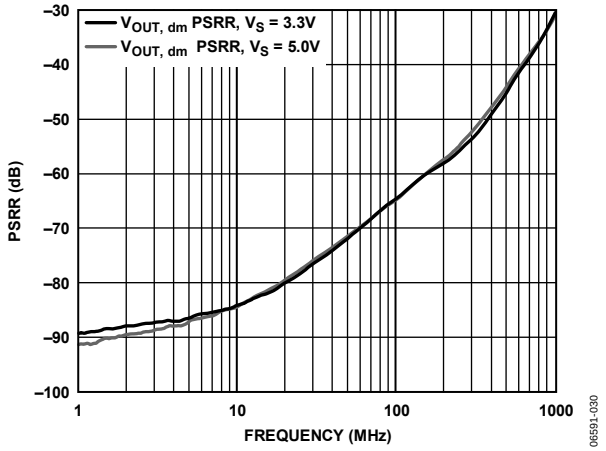


Figure 29. PSRR vs. Frequency, R_L = 200 Ω

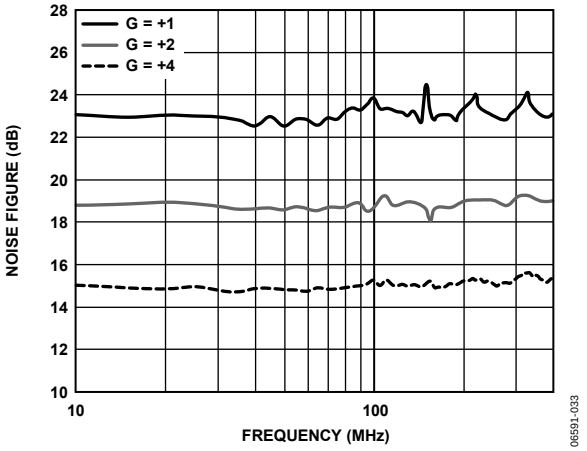


Figure 32. Noise Figure vs. Frequency

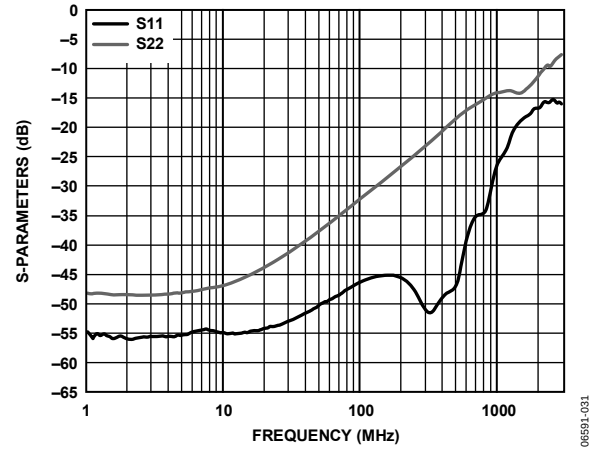


Figure 30. Return Loss (S_{11}, S_{22}) vs. Frequency

Figure 33. Overdrive Recovery Time (Pulse Input)

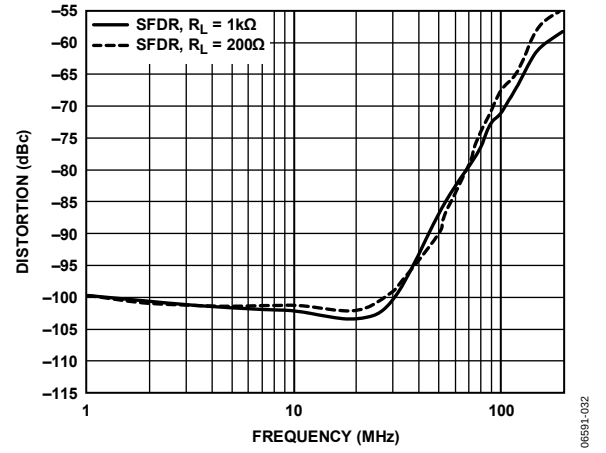


Figure 31. Spurious-Free Dynamic Range vs. Frequency and Load

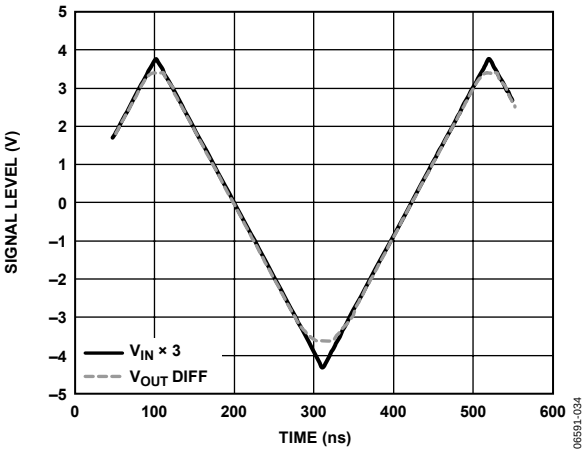


Figure 34. Overdrive Amplitude Characteristics (Triangle Wave Input)

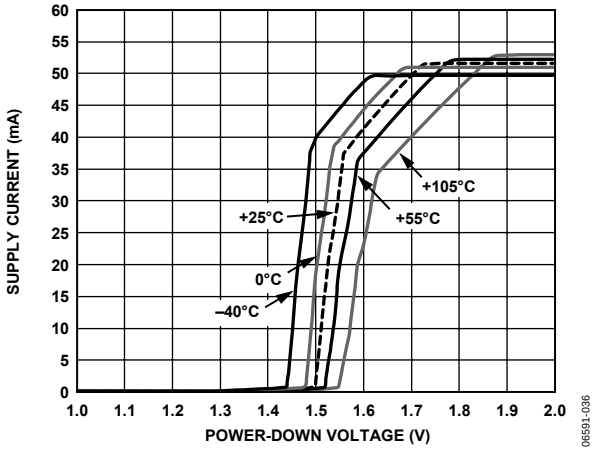


Figure 35. Supply Current vs. $\overline{PD}$ for Various Temperatures

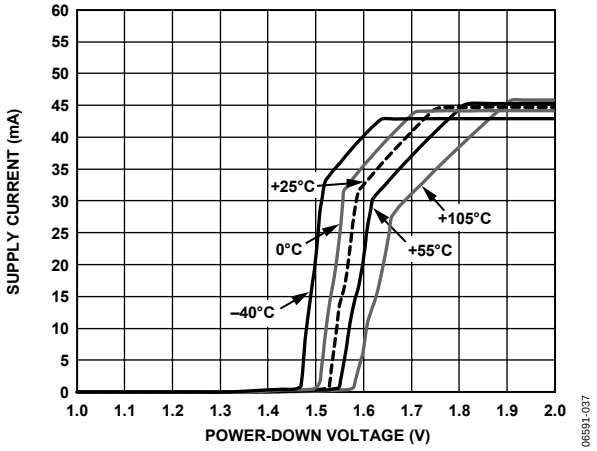


Figure 38. Supply Current vs. $\overline{PD}$ for Various Temperatures, V_S = 3.3 V

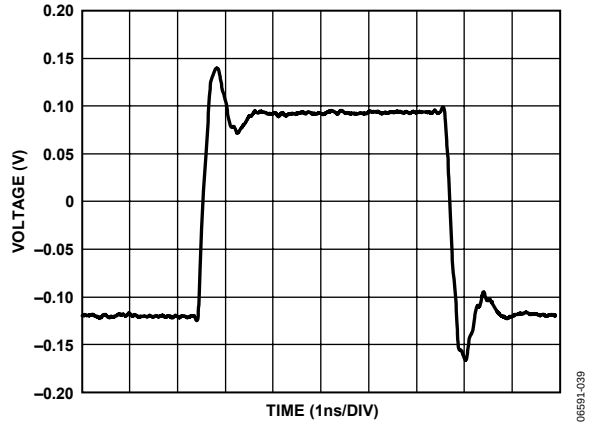


Figure 36. Small Signal Pulse Response

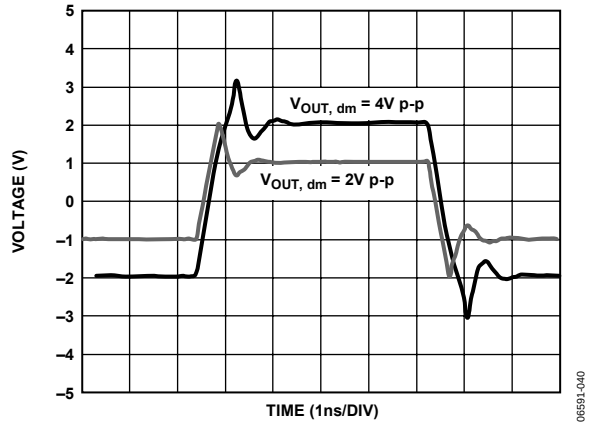


Figure 39. Large Signal Pulse Response

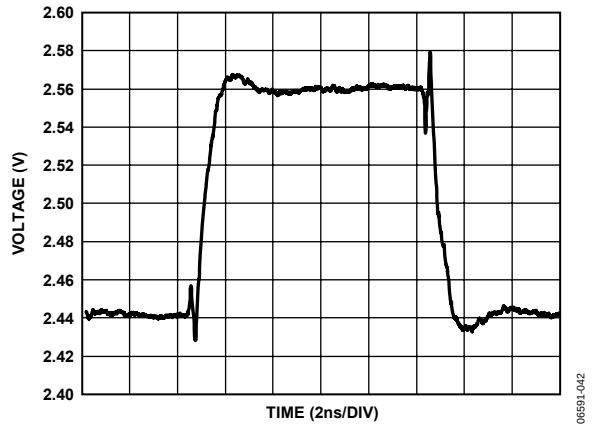


Figure 37. Small Signal V_{OCM} Pulse Response

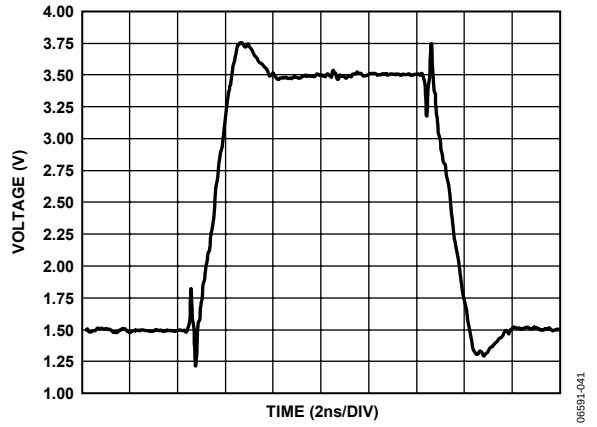


Figure 40. Large Signal V_{OCM} Pulse Response

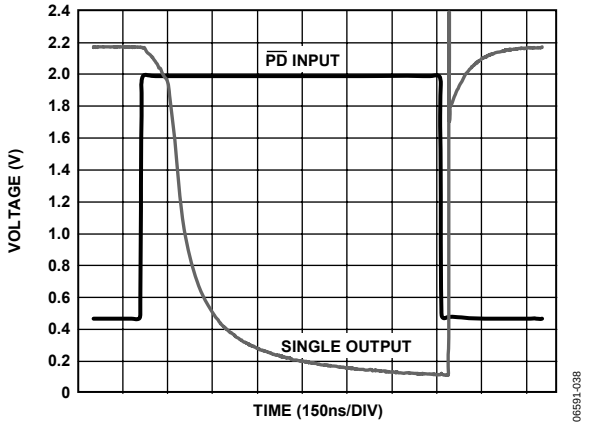


Figure 41. $\overline{PD}$ Response vs. Time

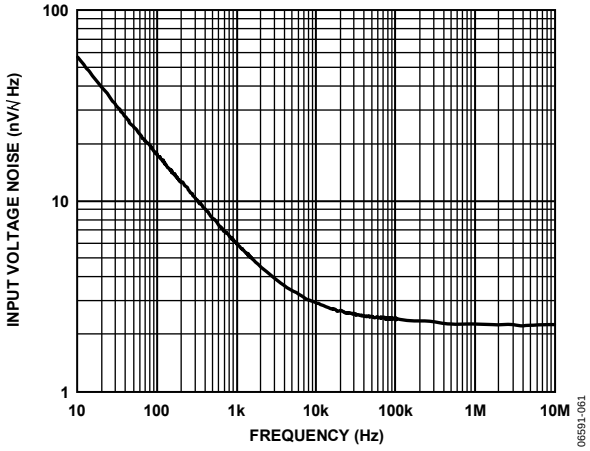


Figure 42. Voltage Spectral Noise Density, RTI

TEST CIRCUITS

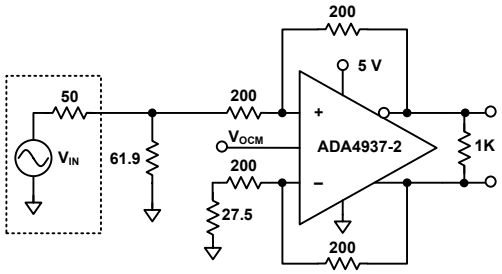


Figure 43. Equivalent Basic Test Circuit

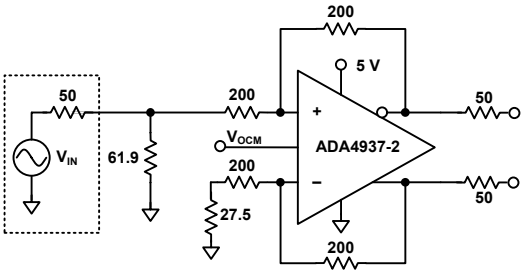


Figure 44. Test Circuit for Output Balance

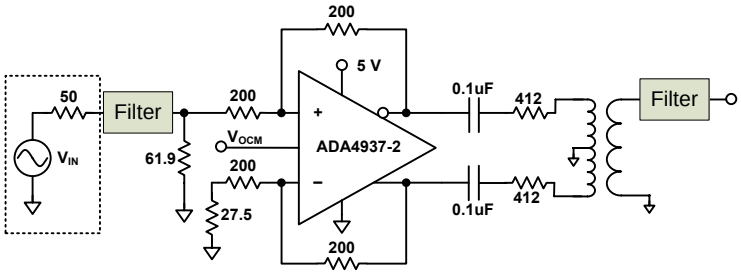


Figure 45. Test Circuit for Distortion Measurements

OPERATIONAL DESCRIPTION

DEFINITION OF TERMS

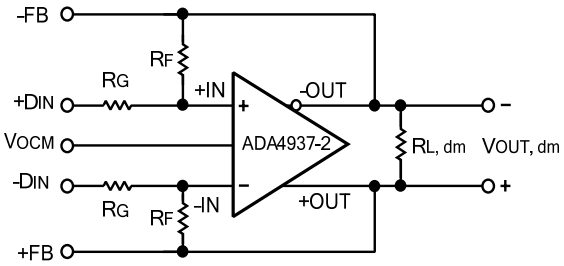


Figure 46. Circuit Definitions

Differential Voltage

This refers to the difference between two node voltages. For example, the output differential voltage (or equivalently, output differential-mode voltage) is defined as

$$V_{OUT,\,dm} = (V_{+OUT} - V_{-OUT})$$

where V_{+OUT} and V_{-OUT} refer to the voltages at the +OUT and −OUT terminals with respect to a common reference.

Common-Mode Voltage

This refers to the average of two node voltages. The output common-mode voltage is defined as

$$V_{OUT,\,cm} = (V_{+OUT} + V_{-OUT})/2$$

Balance

Balance is a measure of how well differential signals are matched in amplitude and are exactly 180° apart in phase. Balance is most easily determined by placing a well-matched resistor divider between the differential voltage nodes and comparing the magnitude of the signal at the divider's midpoint with the magnitude of the differential signal (see Figure 44). By this definition, output balance is the magnitude of the output common-mode voltage divided by the magnitude of the output differential mode voltage.

$$Output\ Balance\ Error = \left| \frac{V_{OUT,\,cm}}{V_{OUT,\,dm}} \right|$$

THEORY OF OPERATION

The ADA4937-2 differs from conventional op amps in that it has two outputs whose voltages move in opposite directions. Like an op amp, it relies on open-loop gain and negative feedback to force these outputs to the desired voltages. The ADA4937-2 behaves much like a standard voltage feedback op amp and makes it easier to perform single-ended-to-differential conversions, common-mode level shifting, and amplifications of differential signals. Also like an op amp, the ADA4937-2 has high input impedance and low output impedance.

Two feedback loops are employed to control the differential and common-mode output voltages. The differential feedback, set with external resistors, controls only the differential output voltage. The common-mode feedback controls only the common-mode output voltage. This architecture makes it easy to set the output common-mode level to any arbitrary value. It is forced, by internal common-mode feedback, to be equal to the voltage applied to the V_{OCM} input, without affecting the differential output voltage.

The ADA4937-2 architecture results in outputs that are highly balanced over a wide frequency range without requiring tightly matched external components. The common-mode feedback loop forces the signal component of the output common-mode voltage to zero. This results in nearly perfectly balanced differential outputs that are identical in amplitude and are exactly 180°5apart in phase.

ANALYZING AN APPLICATION CIRCUIT

The ADA4937-2 uses open-loop gain and negative feedback to force its differential and common-mode output voltages in such a way as to minimize the differential and common-mode error voltages. The differential error voltage is defined as the voltage between the differential inputs labeled +IN and −IN (see Figure 46). For most purposes, this voltage can be assumed to be zero. Similarly, the difference between the actual output common-mode voltage and the voltage applied to V_{OCM} can also be assumed to be zero. Starting from these two assumptions, any application circuit can be analyzed.

SETTING THE CLOSED-LOOP GAIN

The differential-mode gain of the circuit in Figure 46 can be determined by

$$\left|\frac{V_{OUT,dm}}{V_{IN,dm}}\right| = \frac{R_F}{R_G}$$

This assumes the input resistors (R_G) and feedback resistors (R_F) on each side are equal.

ESTIMATING THE OUTPUT NOISE VOLTAGE

The differential output noise of the ADA4937-2 can be estimated using the noise model in Figure 47. The input-referred noise voltage density, v_{nIN}, is modeled as a differential input, and the noise currents, i_{nIN-} and i_{nIN+}, appear between each input and ground. The noise currents are assumed to be equal and produce a voltage across the parallel combination of the gain and feedback resistances. v_{nCM} is the noise voltage density at the V_{OCM} pin. Each of the four resistors contributes $(4kTR_x)^{1/2}$. Table 8 summarizes the input noise sources, the multiplication factors, and the output-referred noise density terms.

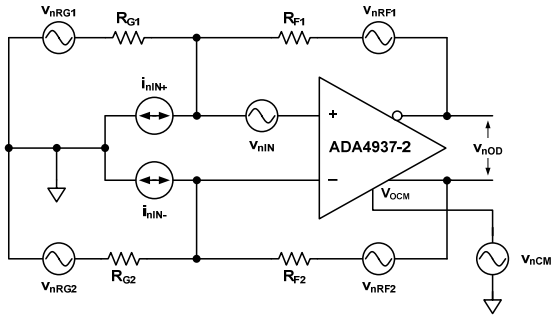


Figure 47. ADA4937-2 Noise Model

Table 8. Output Noise Voltage Density Calculations

Input Noise Contribution	Input Noise Term	Input Noise Voltage Density	Output Multiplication Factor	Output Noise Voltage Density Term
Differential Input	v_{nIN}	v_{nIN}	G_N	$v_{nO1} = G_N(v_{nIN})$
Inverting Input	i_{nIN-}	$i_{nIN-} \times (R_{G2}\|\|R_{F2})$	G_N	$v_{nO2} = G_N[i_{nIN-} \times (R_{G2}\|\|R_{F2})]$
Noninverting Input	i_{nIN+}	$i_{nIN+} \times (R_{G1}\|\|R_{F1})$	G_N	$v_{nO3} = G_N[i_{nIN+} \times (R_{G1}\|\|R_{F1})]$
V_{OCM} Input	v_{nCM}	v_{nCM}	$G_N(\beta_1 - \beta_2)$	$v_{nO4} = G_N(\beta_1 - \beta_2)(v_{nCM})$
Gain Resistor R_{G1}	v_{nRG1}	$(4kTR_{G1})^{1/2}$	$G_N(1 - \beta_2)$	$v_{nO5} = G_N(1 - \beta_2)(4kTR_{G1})^{1/2}$
Gain Resistor R_{G2}	v_{nRG2}	$(4kTR_{G2})^{1/2}$	$G_N(1 - \beta_1)$	$v_{nO6} = G_N(1 - \beta_1)(4kTR_{G2})^{1/2}$
Feedback Resistor R_{F1}	v_{nRF1}	$(4kTR_{F1})^{1/2}$	1	$v_{nO7} = (4kTR_{F1})^{1/2}$
Feedback Resistor R_{F2}	v_{nRF2}	$(4kTR_{F2})^{1/2}$	1	$v_{nO8} = (4kTR_{F2})^{1/2}$

Similar to the case of a conventional op amp, the output noise voltage densities can be estimated by multiplying the input-referred terms at +IN and −IN by the appropriate output factor,

where:

$G_N = \frac{2}{(\beta_1 + \beta_2)}$ is the circuit noise gain.

$\beta_1 = \frac{R_{G1}}{R_{F1} + R_{G1}}$ and $\beta_2 = \frac{R_{G2}}{R_{F2} + R_{G2}}$ are the feedback factors.

When $R_{F1}/R_{G1} = R_{F2}/R_{G2}$, then $\beta 1 = \beta 2 = \beta$, and the noise gain becomes

$$G_N = \frac{1}{\beta} = 1 + \frac{R_F}{R_G}$$

Note that the output noise from V_{OCM} goes to zero in this case. The total differential output noise density, v_{nOD}, is the root-sum-square of the individual output noise terms.

$$v_{nOD} = \sqrt{\sum_{i=1}^{8} v_{nOi}^2}$$

THE IMPACT OF MISMATCHES IN THE FEEDBACK NETWORKS

As previously mentioned, even if the external feedback networks (R_F/R_G) are mismatched, the internal common-mode feedback loop still forces the outputs to remain balanced. The amplitudes of the signals at each output remain equal and 180° out of phase. The input-to-output, differential mode gain varies proportionately to the feedback mismatch, but the output balance is unaffected.

As well as causing a noise contribution from V_{OCM}, ratio matching errors in the external resistors result in a degradation of the ability of the circuit to reject input common-mode signals, much the same as for a four-resistor difference amplifier made from a conventional op amp.

In addition, if the dc levels of the input and output common-mode voltages are different, matching errors result in a small differential-mode output offset voltage. When G = 1, with a ground referenced input signal and the output common-mode level set to 2.5 V, an output offset of as much as 25 mV (1% of the difference in common-mode levels) can result if 1% tolerance resistors are used. Resistors of 1% tolerance result in a worst-case input CMRR of about 40 dB, a worst-case differential-mode output offset of 25 mV due to 2.5 V level-shift, and no significant degradation in output balance error.

CALCULATING THE INPUT IMPEDANCE OF AN APPLICATION CIRCUIT

The effective input impedance of a circuit depends on whether the amplifier is being driven by a single-ended or differential signal source. For balanced differential input signals, as shown in Figure 48, the input impedance ($R_{IN, dm}$) between the inputs ($+D_{IN}$ and $-D_{IN}$) is simply $R_{IN, dm} = 2 \times R_G$.

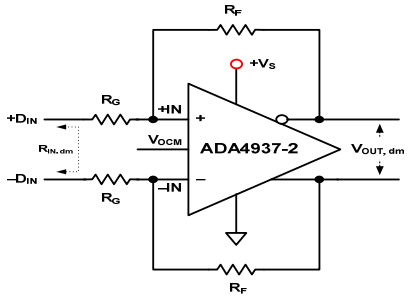


Figure 48. ADA4937-2 Configured for Balanced (Differential) Inputs

For an unbalanced, single-ended input signal (see Figure 49), the input impedance is

$$R_{IN,cm} = \left(\frac{R_G}{1 - \frac{R_F}{2 \times (R_G + R_F)}} \right)$$

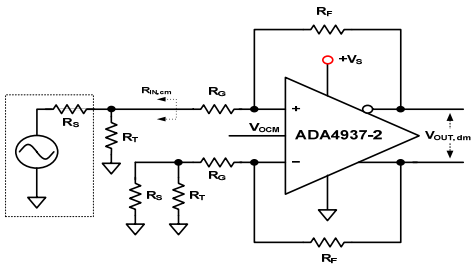


Figure 49. ADA4937-2 Configured for Unbalanced (Single-Ended) Input

The input impedance of the circuit is effectively higher than it would be for a conventional op amp connected as an inverter because a fraction of the differential output voltage appears at the inputs as a common-mode signal, partially bootstrapping the voltage across the input resistor R_G.

INPUT COMMON-MODE VOLTAGE RANGE IN SINGLE-SUPPLY APPLICATIONS

The ADA4937-2 is optimized for level-shifting, ground-referenced input signals. As such, the center of the input common-mode range is shifted approximately 1 V down from midsupply. For 5 V single-supply operation, the input common-mode range at the summing nodes of the amplifier is 0.3 V to 3.0 V, and 0.3 V to 1.9 V with a 3.3 V supply. To avoid clipping at the outputs, the voltage swing at the +IN and –IN terminals must be confined to these ranges.

SETTING THE OUTPUT COMMON-MODE VOLTAGE

The V_{OCM} pin of the ADA4937-2 is internally biased at a voltage approximately equal to the midsupply point (average value of the voltages on V+ and V−). Relying on this internal bias results in an output common-mode voltage that is within about 100 mV of the expected value.

In cases where more accurate control of the output common-mode level is required, it is recommended that an external source, or resistor divider (10 kΩ or greater resistors), be used. The output common-mode offset listed in the Specifications

section assumes that the V_{OCM} input is driven by a low impedance voltage source.

It is also possible to connect the V_{OCM} input to a common-mode level (CML) output of an ADC. However, care must be taken to assure that the output has sufficient drive capability. The input impedance of the V_{OCM} pin is approximately 10 kΩ. If multiple ADA4937-2 devices share one reference output, it is recommended that a buffer be used.

Table 9 and Table 10 list several common gain settings, associated resistor values, input impedance, output noise density, and approximate large signal bandwidth for both balanced and unbalanced input configurationns. Also shown are the input common-mode voltage swings under the given conditions for different V_{OCM} settings with single 5 V and 3.3 V supplies.

Note that some gain configurations at 3.3 V cause the input common-mode voltage to exceed the specified range and should be avoided. If larger gains are required, other alternatives should be considered, such as an input common-mode offset, ac coupling, or a bipolar power supply.

Table 9. Differential Ground-Referenced Input, DC-Coupled; See Figure 48

Nominal Gain (dB)	R_F (Ω)	R_G (Ω)	$R_{IN, dm}$(Ω)	Differential Output Noise Density (nV/√Hz)	Approximate Large-Signal Bandwidth (MHz) $+V_S$ = 5 V/3.3 V	Common-Mode Swing at +IN, –IN (V)			
						$+V_S$ = 5 V, $V_{OUT, dm}$ = 2.0 V p-p		$+V_S$ = 3.3 V, $V_{OUT, dm}$ = 1.6 V p-p	
						V_{OCM} = 2.5 V	V_{OCM} = 3.2 V	V_{OCM} = 1.6 V	V_{OCM} = 1.8 V
0	200	200	400	5.8	1500/1100	0.75 to 1.75	1.10 to 2.10	0.40 to 1.20	0.50 to 1.30
	348	348	696	6.7					
3	280	200	400	7.2	1500/1100	0.69 to 1.40	0.98 to 1.69	0.39 to 1.04	0.46 to 1.04
	348	249	498	7.6					
6	200	100	200	8.0	1400/1100	0.58 to 1.08	0.82 to 1.32	0.33 to 0.73	0.40 to 0.80
	348	174	348	9.0					
10	316	100	200	11	800/700	0.44 to 0.76	0.61 to 0.92	Out of range	0.31 to 0.56
	348	110	220	12					
12	402	100	200	14	500/500	0.37 to 0.62	0.51 to 0.76	Out of range	Out of range
	348	86.6	173	13					
14	499	100	200	17	300/300	0.32 to 0.52	0.43 to 0.63	Out of range	Out of range
	348	69.8	140	16					

Table 10. Single-Ended Ground-Referenced Input, DC-Coupled, R_S = 50 Ω; See Figure 49

Nominal Gain (dB)	R_F (Ω)	R_{G1} (Ω)	R_T (Ω)	$R_{IN,cm}$ (Ω)	R_{G2} (Ω)[1]	Differential Output Noise Density (nV/√Hz)	Approximate Large-Signal Bandwidth (MHz) $+V_S$ = 5 V/3.3 V	Common-Mode Swing at +IN, -IN (V)			
								$+V_S$ = 5 V, $V_{OUT,dm}$ = 2.0 V p-p		$+V_S$ = 3.3 V, $V_{OUT,dm}$ = 1.6 V p-p	
								V_{OCM} = 2.5 V	V_{OCM} = 3.2 V	V_{OCM} = 1.6 V	V_{OCM} = 1.8 V
0	200	200	61.9	267	226	5.5	1500/1100	0.75 to 1.75	1.13 to 2.26	0.40 to 1.30	Out of range
	348	348	56.2	464	374	6.5					
3	280	200	60.4	282	226	6.8	1500/1100	0.71 to 1.52	1.03 to 1.83	0.39 to 1.04	0.48 to 1.13
	348	249	59.0	351	274	7.3					
6	200	100	75.0	150	130	7.0	1400/1100	0.66 to 1.31	0.94 to 1.59	0.37 to 0.89	0.45 to 0.97
	348	174	61.9	261	200	8.4					
10	316	100	73.2	161	130	9.7	800/700	0.52 to 0.93	0.73 to 1.14	0.30 to 0.63	0.36 to 0.69
	348	110	69.8	177	140	10					
12	402	100	71.5	167	130	12	500/500	0.45 to 0.77	0.62 to 0.94	Out of range	0.31 to 0.57
	348	86.6	76.8	144	118	11					
14	499	100	71.5	171	130	14	300/300	0.39 to 0.65	0.53 to 0.79	Out of range	Out of range
	348	69.8	86.6	120	100	12					

[1] $R_{G2} = R_{G1} + (R_S||R_T)$

3.3 V OPERATION

The ADA4937-2 provides excellent performance in 3.3 V single-supply applications. Significant power savings can be realized when the ADA4937-2 is used in combination with a low voltage ADC.

The circuit in **Error! Reference source not found.** is an example of the ADA4937-2 driving an AD9230, 12-bit, 250 MSPS ADC that is specified to operate with a single 1.8 V supply. The performance of the ADC is optimized when it is driven differentially, making the best use of the signal swing available within the 1.8 V supply. The ADA4937-2 performs the single-ended-to-differential conversion, common-mode level-shifting, and buffering of the driving signal.

The ADA4937-2 is configured with a single 3.3 V supply and a gain of 2 V/V for a single-ended input to differential output. The 59 Ω termination resistor, in parallel with the single-ended input impedance of 306 Ω, provides a 50 Ω termination for the source. The additional 26 Ω (226 Ω total) at the inverting input balances the parallel impedance of the 50 Ω source and termination resistor driving the noninverting input.

The signal generator has a symmetric, ground-referenced bipolar output. The V_{OCM} pin is connected to the CML output of the AD9230, and sets the output common mode of the ADA4937-2 at 1.4 V. One-third of the output common-mode voltage of the amplifier is fed back to the summing nodes, biasing –IN and + IN at ~ 0.5 V. For a common-mode voltage of 1.4 V, each ADA4937-2 output swings between 1.09 V and 1.71 V, providing a 1.25 V p-p differential output.

A third-order, 125 MHz, low-pass filter between the ADA4937-2 and the AD9230 reduces the noise bandwidth of the amplifier and isolates the driver outputs from the ADC inputs.

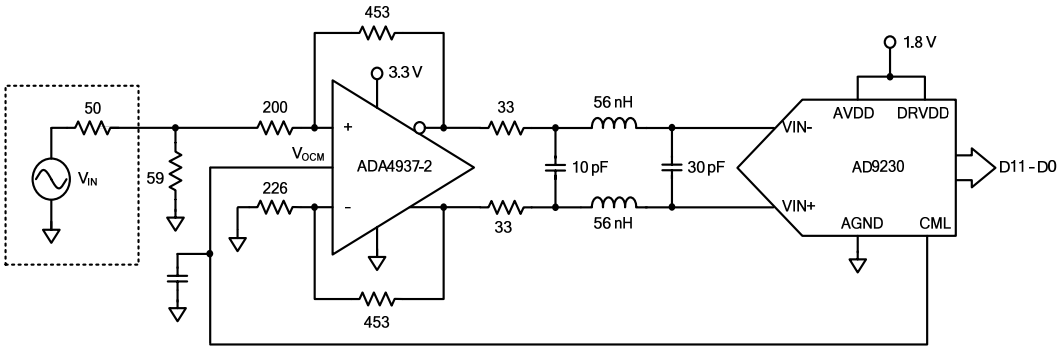
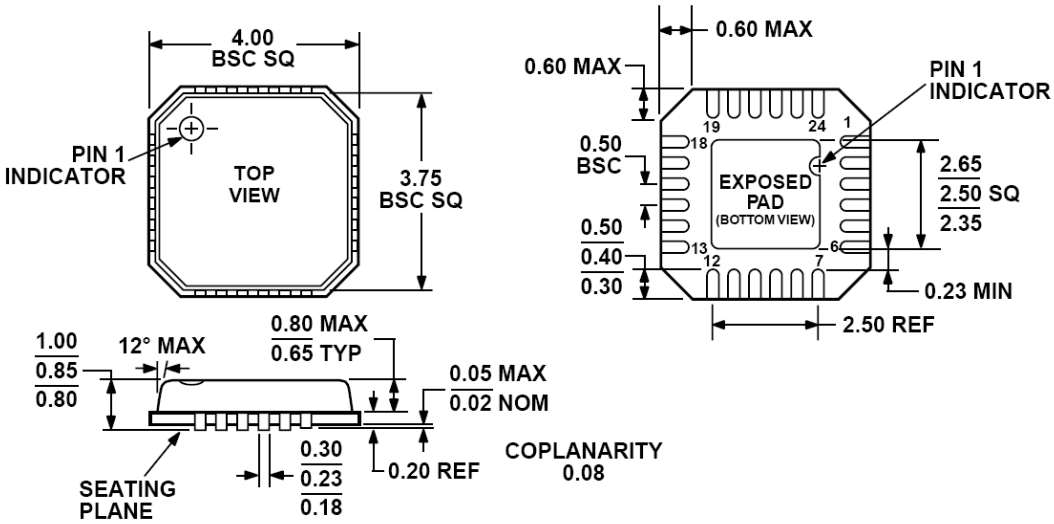


Figure 50. ADA4937-2 Driving an AD9230, a 12-Bit, 250 MSPS ADC

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-VGGD-8

Figure 5124-Lead Lead Frame Chip Scale Package [LFCSP-VQ]
4mm x 4mm Body Very Thin Quad
(CP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Ordering Quantity	
ADA4937-2YCPZ-R2[1]	–40°C to +105°C	24-Lead LFCSP_VQ	CP-24-3	5,000	
ADA4937-2YCPZ-RL[1]	–40°C to +105°C	24-Lead LFCSP_VQ	CP-24-3	1,500	
ADA4937-2YCPZ-R7[1]	–40°C to +105°C	24-Lead LFCSP_VQ	CP-24-3	250	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

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